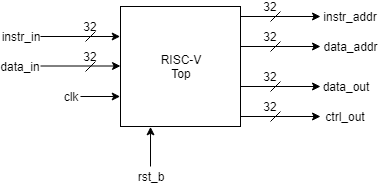
RISC-V Top



# Description

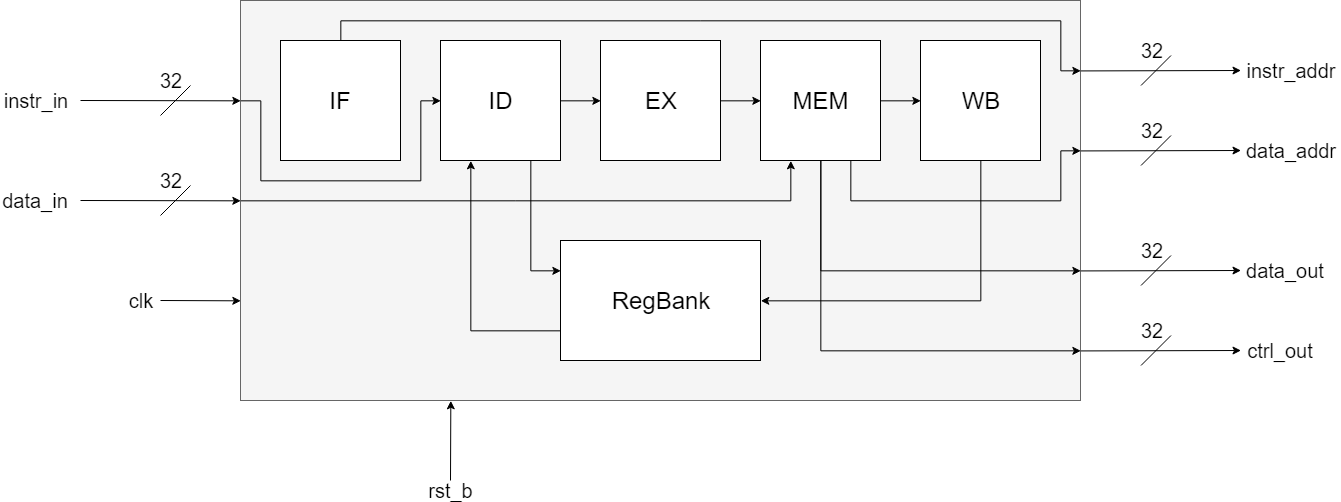
This is the RISC-V Processor’s top-level module. This is a 32-bit single cycle processor following the RISC-V specification (<https://riscv.org/specifications/>). It implements the RV32I (Base Integer ISA). It features 32x-32bit registers (where register 0 (x0) is tied to ground) and the ability to process additions, subtractions, shift operations, logical operations, conditional and unconditional branch operations and load/store operations.

Documentation on installing and using the compilers can be found in the “Documentation” folder. Follow links attached to sub-module names to locate their documentation, alternatively go to the “Documentation” folder.

# Data Dictionary

|  |  |
| --- | --- |
| **Signal Name** | **Description** |
| clk | Clock input for the RISC-V Processor |
| rst\_b | Reset input for the RISC-V Processor |
| instr\_in | Instruction coming from memory |
| data\_in | Data coming from memory |
| instr\_addr | Current value of the program counter |
| data\_addr | Data address pointer for memory |
| data\_out | Output data for memory |
| ctrl\_out | Memory control signals |

# Architecture



This processor follows a 5-stage architecture as shown:

* [**IF:**](RISC-V%20IF.docx) Instruction Fetch Module, retrieves the next instruction from memory.
* [**ID:**](RISC-V%20ID.docx) Instruction Decode Module, decodes the instruction and retrieves register values from register bank.
* **EX:** Execution Module, executes instructions based on the information decoded and the data given.
* **MEM:** Memory Management Module, handles writing and reading from memory and byte, halfword and word load/store operations/
* **WB:** Write Back Module, handles writing back the result of the instruction to the register bank.
* **RegBank:** Register Bank Module, where the 32x32-bit registers are stored.

This 5-stage architecture will then lead into a pipelined architecture increases the processors efficiency by approx. 67%.

# Revision History

* Revision 0.01 – Initial Revision, created document with block diagram, module description and data dictionary